TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55VCM216ASTN is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 40 ns. It is automatically placed in low-power mode at 0.7 μA standby current (at V_{DD} = 3 V, Ta = 25°C, typical) when chip enable ($\overline{CE1}$) is asserted high or (CE2) is asserted low. There are three control inputs. $\overline{CE1}$ and CE2 are used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of −40° to 85°C, the TC55VCM216ASTN can be used in environments exhibiting extreme temperature conditions. The TC55VCM216ASTN is available in a plastic 48-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
  Operating: 9 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6 V
- Power down features using $\overline{CE1}$ and CE2
- Data retention supply voltage of 1.5 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of −40° to 85°C
- Standby Current (maximum):

3.6 V	10 μA
3.0 V	5 μA

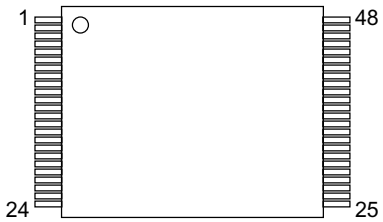
- Access Times (maximum):

	TC55VCM216ASTN	
	40	55
Access Time	40 ns	55 ns
$\overline{CE1}$ Access Time	40 ns	55 ns
CE2 Access Time	40 ns	55 ns
$\overline{OE}$ Access Time	25 ns	30 ns

- Package:
  TSOP I 48-P-1214-0.50 (Weight:0.35 g typ)

PIN ASSIGNMENT (TOP VIEW)

48 PIN TSOP



(Normal)

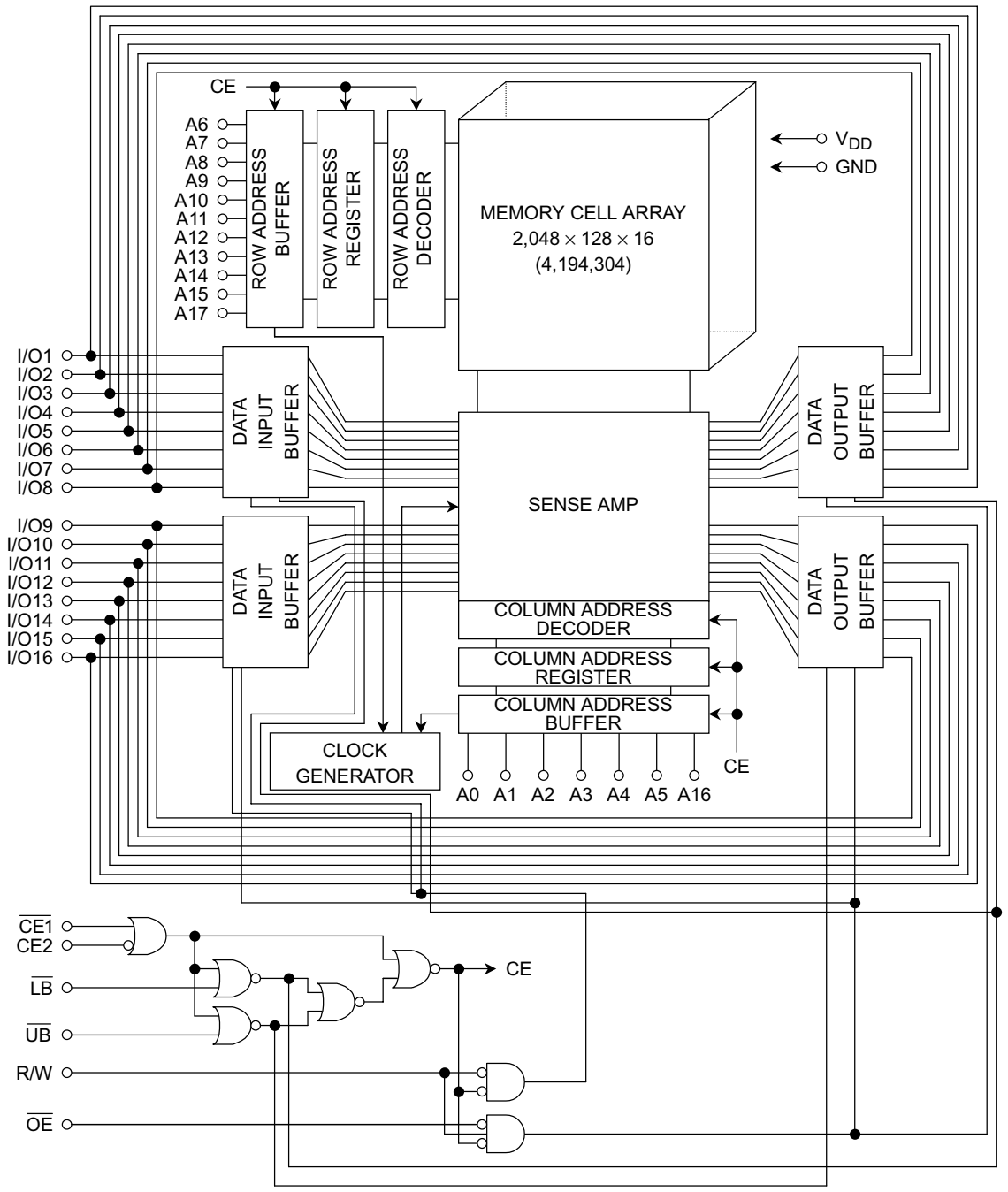
PIN NAMES

A0~A17	Address Inputs
$\overline{CE1}$, CE2	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground
NC	No Connection
OP*	Option

*: OP pin must be open or connected to GND.

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A15	A14	A13	A12	A11	A10	A9	A8	NC	NC	R/W	CE2	OP	$\overline{UB}$	$\overline{LB}$	NC
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A17	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{CE1}$	GND	$\overline{OE}$	I/O1	I/O9	I/O2	I/O10
Pin No.	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Pin Name	I/O3	I/O11	I/O4	I/O12	V_{DD}	I/O5	I/O13	I/O6	I/O14	I/O7	I/O15	I/O8	I/O16	GND	NC	A16

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	H	L	H	L	L	Output	Output	I_{DDO}
	L	H	L	H	H	L	High-Z	Output	I_{DDO}
	L	H	L	H	L	H	Output	High-Z	I_{DDO}
Write	L	H	*	L	L	L	Input	Input	I_{DDO}
	L	H	*	L	H	L	High-Z	Input	I_{DDO}
	L	H	*	L	L	H	Input	High-Z	I_{DDO}
Output Deselect	L	H	H	H	L	L	High-Z	High-Z	I_{DDO}
	L	H	H	H	H	L	High-Z	High-Z	I_{DDO}
	L	H	H	H	L	H	High-Z	High-Z	I_{DDO}
Standby	H	*	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	L	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	*	*	*	H	H	High-Z	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	−0.3~4.2	V
V_{IN}	Input Voltage	−0.3*~4.2	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

*: −2.0 V when measured at a pulse width of 20ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = −40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage		2.3	—	3.6	V
V_{IH}	Input High Voltage	V_{DD} = 2.3 V~2.7 V	2.0	—	V_{DD} + 0.3	V
		V_{DD} = 2.7 V~3.6 V	2.2			
V_{IL}	Input Low Voltage		−0.3*	—	V_{DD} × 0.24	V
V_{DH}	Data Retention Supply Voltage		1.5	—	3.6	V

*: −2.0 V when measured at a pulse width of 20ns

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 2.3 to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{DD}				—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} – 0.5 V				–0.5	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V				2.1	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{LB}$ = $\overline{UB}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V~V_{DD}				—	—	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, $\overline{LB}$ = $\overline{UB}$ = V_{IL}, I_{OUT} = 0 mA, Other Input = V_{IH}/V_{IL}		t_{cycle}	MIN	—	—	35	mA
					1 μs	—	—	8	
I_{DDO2}		$\overline{CE1}$ = 0.2 V and CE2 = V_{DD} – 0.2 V and R/W = V_{DD} – 0.2 V, $\overline{LB}$ = $\overline{UB}$ = 0.2 V, I_{OUT} = 0 mA, Other Input = V_{DD} – 0.2 V/0.2 V		t_{cycle}	MIN	—	—	30	mA
					1 μs	—	—	3	
I_{DDS1}	Standby Current	1) $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} 2) $\overline{LB}$ = $\overline{UB}$ = V_{IH}				—	—	1	mA
I_{DDS2}		1) $\overline{CE1}$ = V_{DD} – 0.2 V, CE2 = V_{DD} – 0.2 V 2) CE2 = 0.2 V 3) $\overline{LB}$ = $\overline{UB}$ = V_{DD} – 0.2 V, $\overline{CE1}$ = 0.2 V, CE2 = V_{DD} – 0.2 V	V_{DD} = 3.3 V ± 0.3 V	Ta = –40~85°C		—	—	10	μA
			V_{DD} = 3.0 V	Ta = 25°C		—	0.7	—	
				Ta = –40~40°C		—	—	2	
				Ta = –40~85°C		—	—	5	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.7 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55VCM216ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	40	—	55	—	ns
t_{ACC}	Address Access Time	—	40	—	55	
t_{CO1}	Chip Enable($\overline{CE1}$) Access Time	—	40	—	55	
t_{CO2}	Chip Enable(CE2) Access Time	—	40	—	55	
t_{OE}	Output Enable Access Time	—	25	—	30	
t_{BA}	Data Byte Control Access Time	—	40	—	55	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	5	—	5	—	
t_{OD}	Chip Enable High to Output High-Z	—	20	—	25	
t_{ODO}	Output Enable High to Output High-Z	—	20	—	25	
t_{BD}	Data Byte Control High to Output High-Z	—	20	—	25	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55VCM216ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	40	—	55	—	ns
t_{WP}	Write Pulse Width	30	—	40	—	
t_{CW}	Chip Enable to End of Write	35	—	45	—	
t_{BW}	Data Byte Control to End of Write	35	—	45	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	20	—	25	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	20	—	25	—	
t_{DH}	Data Hold Time	0	—	0	—	

Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.3 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55VCM216ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{ACC}	Address Access Time	—	55	—	70	
t_{CO1}	Chip Enable($\overline{CE1}$) Access Time	—	55	—	70	
t_{CO2}	Chip Enable(CE2) Access Time	—	55	—	70	
t_{OE}	Output Enable Access Time	—	30	—	35	
t_{BA}	Data Byte Control Access Time	—	55	—	70	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	5	—	5	—	
t_{OD}	Chip Enable High to Output High-Z	—	25	—	30	
t_{ODO}	Output Enable High to Output High-Z	—	25	—	30	
t_{BD}	Data Byte Control High to Output High-Z	—	25	—	30	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55VCM216ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	
t_{CW}	Chip Enable to End of Write	45	—	55	—	
t_{BW}	Data Byte Control to End of Write	45	—	55	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	25	—	30	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	25	—	30	—	
t_{DH}	Data Hold Time	0	—	0	—	

Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Input pulse level	0.2 V, $V_{DD} \times 0.7$ V + 0.2 V
t_R, t_F	1V / ns(Fig.1)
Timing measurements	$V_{DD} \times 0.5$
Reference level	$V_{DD} \times 0.5$
Output load	30 pF + 1 TTL Gate(Fig.2)

Fig.1 : Input rise and fall time

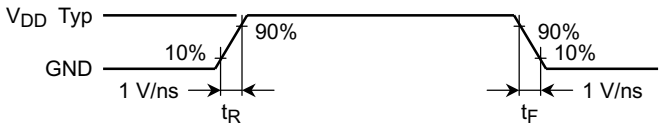
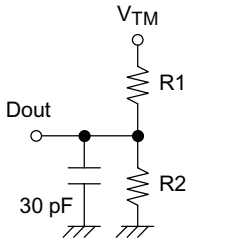


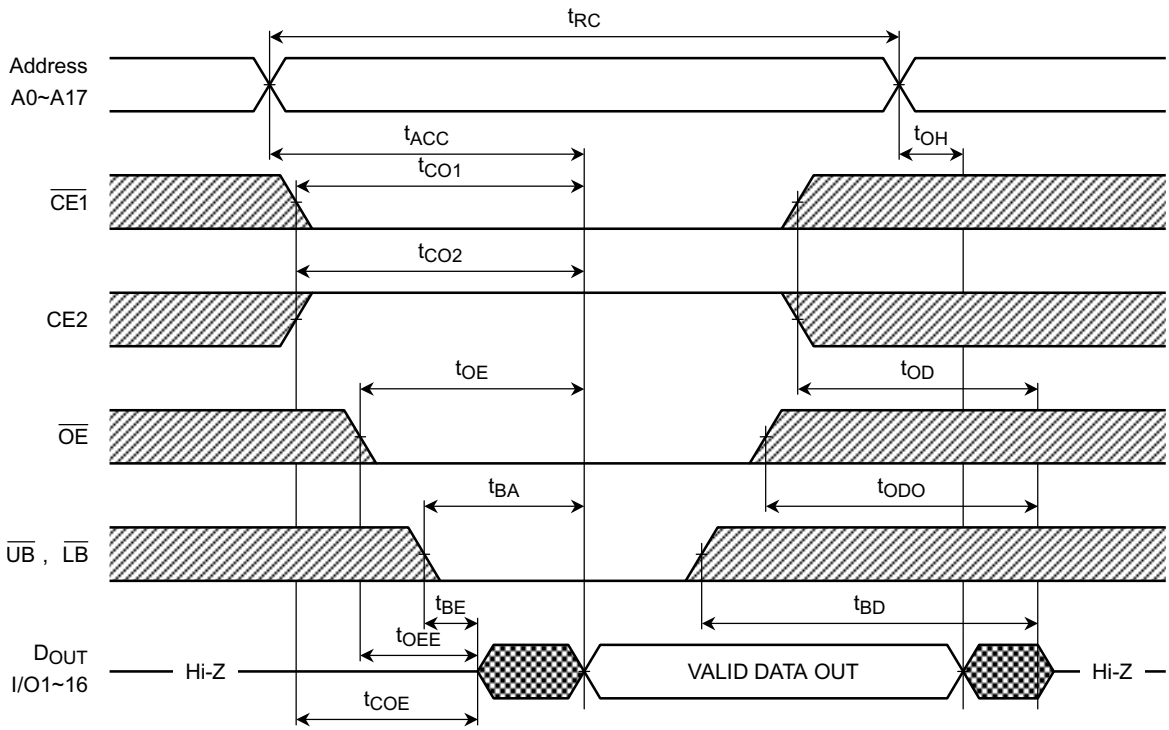
Fig.2 : Output load



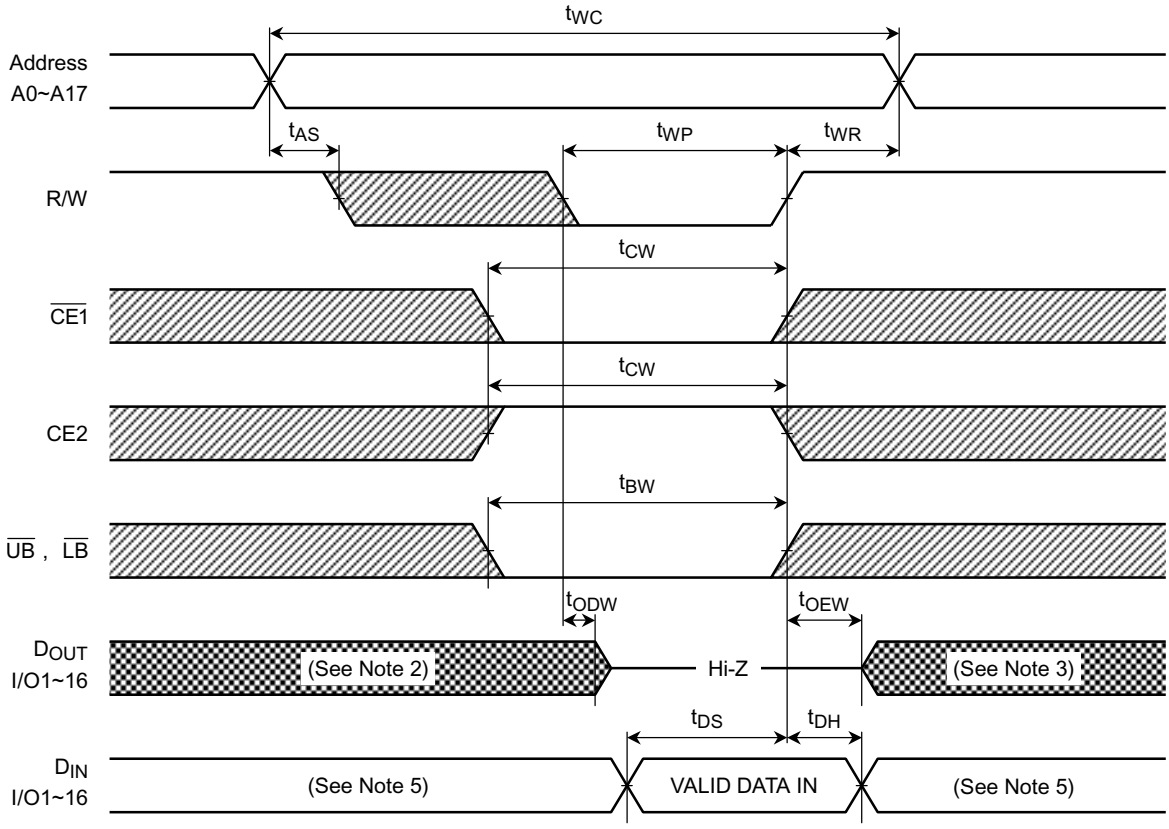
R1 = 810 Ω
R2 = 1610 Ω
V_{TM} = 2.3 V

TIMING DIAGRAMS

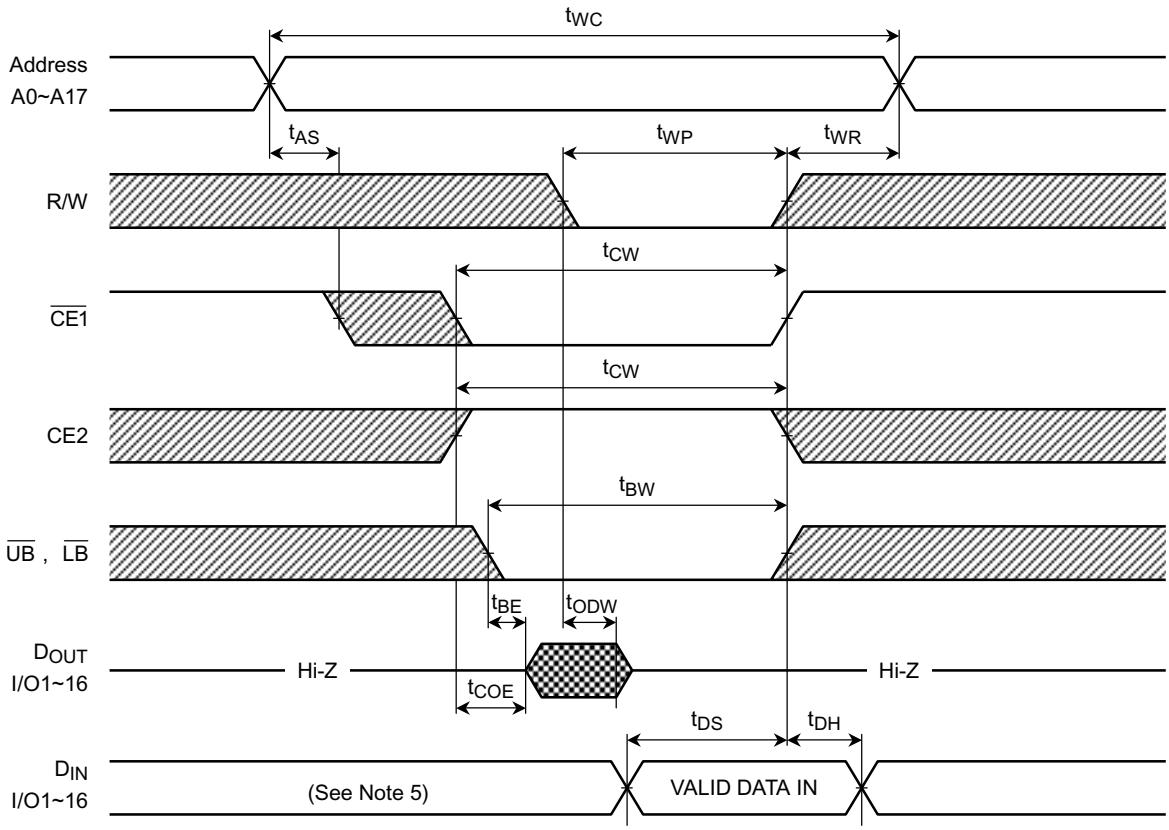
READ CYCLE (See Note 1)



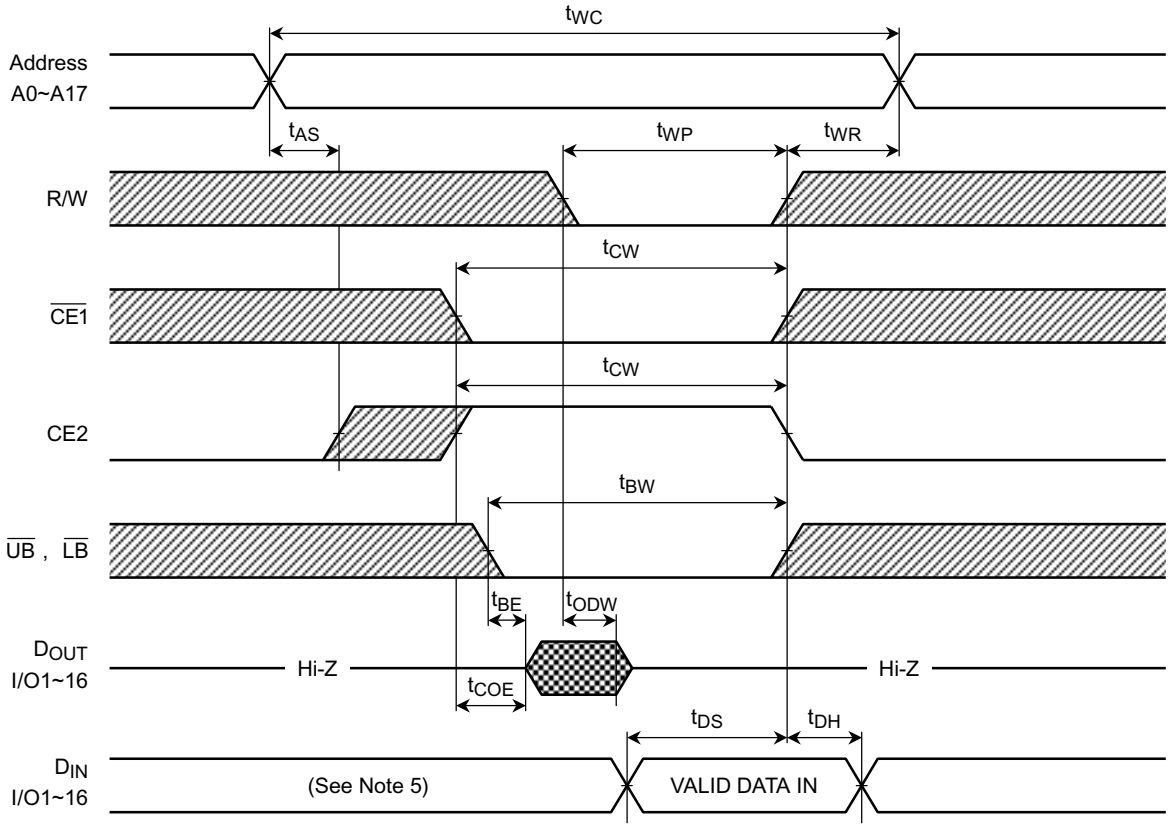
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



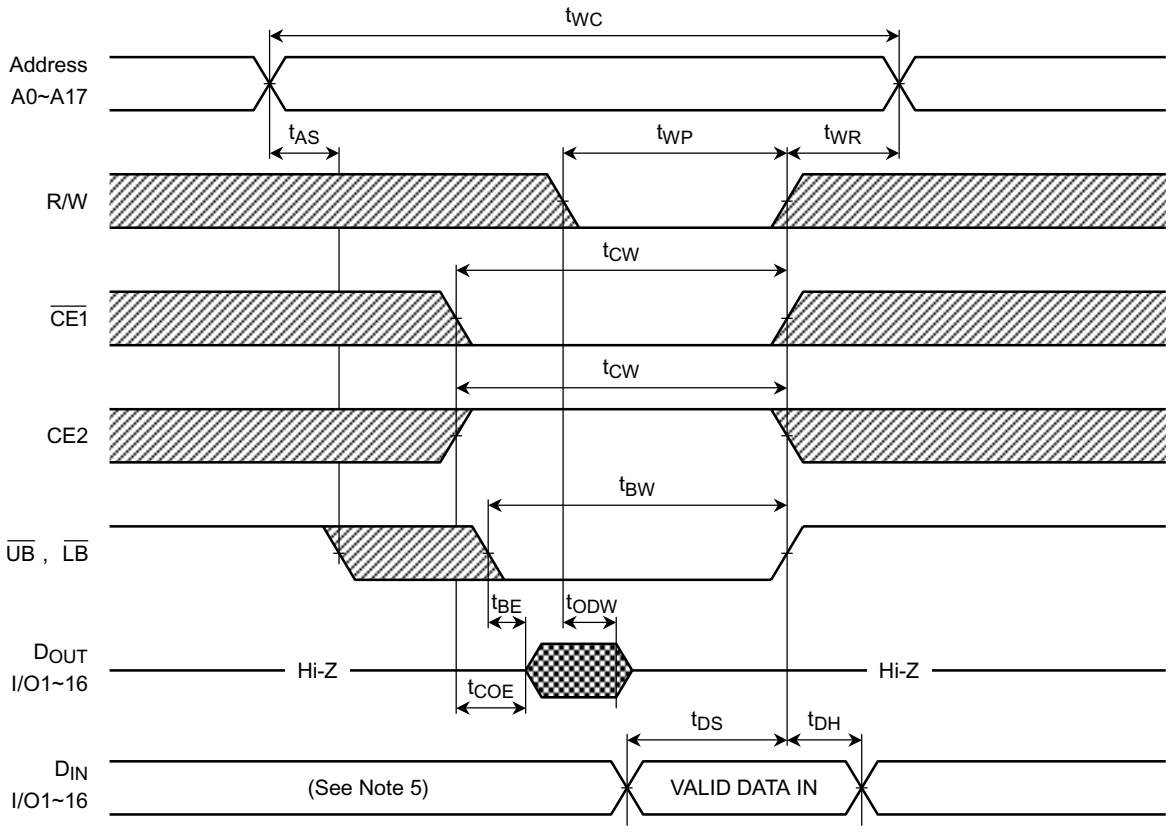
WRITE CYCLE 2 ($\overline{CE1}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



WRITE CYCLE 4 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)



Note:

(1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE1}$ (or $\overline{UB}$ or $\overline{LB}$) goes LOW(or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE1}$ (or $\overline{UB}$ or $\overline{LB}$) goes HIGH(or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

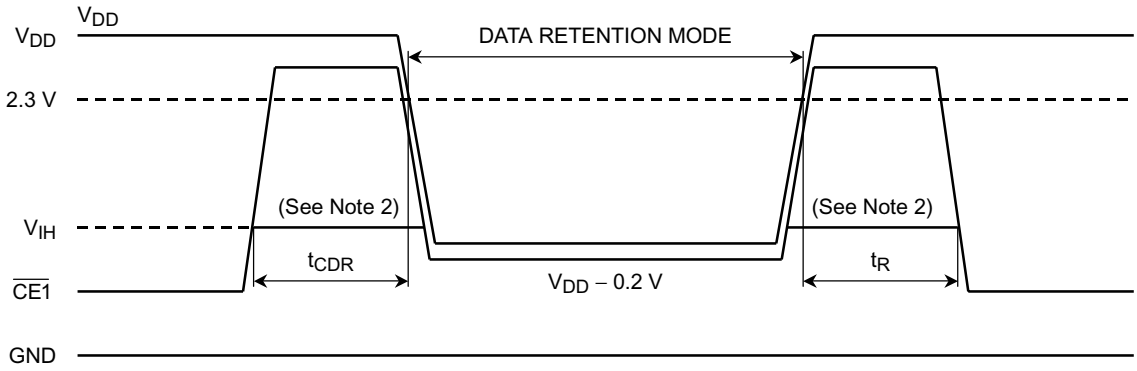
(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

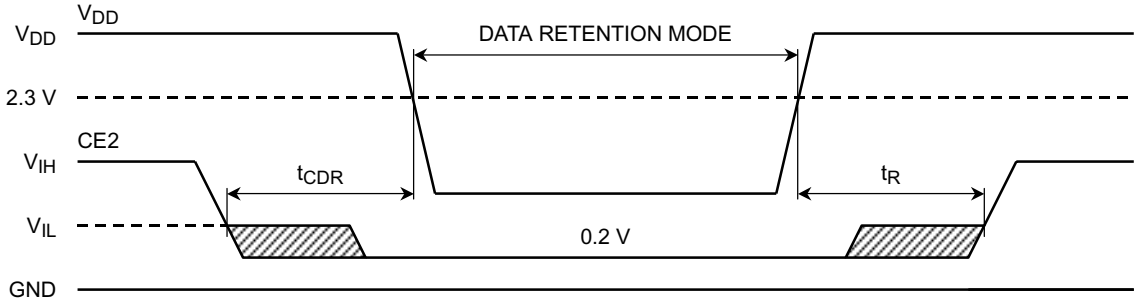
DATA RETENTION CHARACTERISTICS (Ta = –40° to 85°C)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			1.5	—	3.6	V
I_{DDS2}	Standby Current	V_{DH} = 3.6 V	Ta = –40~85°C	—	—	10	μA
		V_{DH} = 3.0 V	Ta = –40~40°C	—	—	2	
			Ta = –40~85°C	—	—	5	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	—	—	ns
t_R	Recovery Time			5	—	—	ms

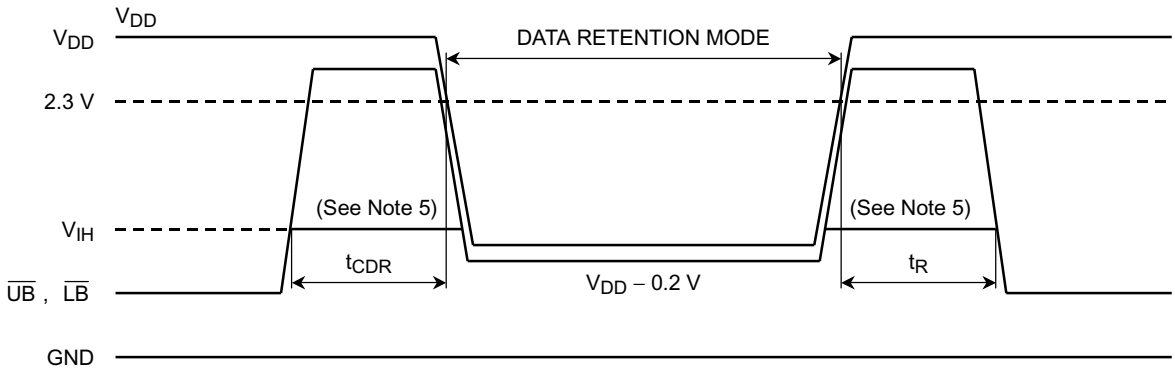
$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



$\overline{UB}$, $\overline{LB}$ CONTROLLED DATA RETENTION MODE (See Note 4)



Note:

(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V or CE2 ≥ V_{DD} − 0.2 V.

(2) When $\overline{CE1}$ is operating at the V_{IH}(min.) level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.3(2.7) to 2.2V(2.4 V).

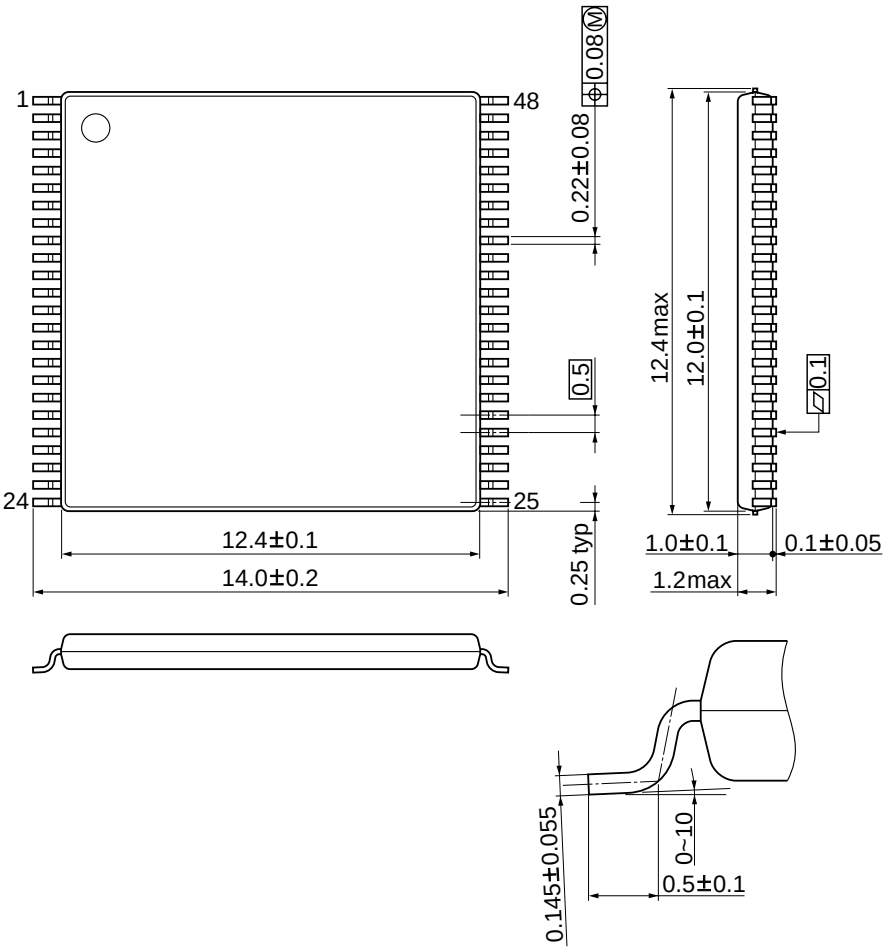
(3) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V.

(4) In $\overline{UB}$ (or $\overline{LB}$) controlled data retention mode, minimum standby current mode is entered when $\overline{CE1}$ ≤ 0.2 V or $\overline{CE1}$ ≥ V_{DD} − 0.2 V, CE2 ≤ 0.2 V or CE2 ≥ V_{DD} − 0.2 V.

(5) When $\overline{UB}$ (or $\overline{LB}$) is operating at the V_{IH}(min.) level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.3(2.7) to 2.2V(2.4 V).

PACKAGE DIMENSIONS

TSOP I 48-P-1214-0.50 Unit:mm



Weight:0.35 g (typ)

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000707EBA

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