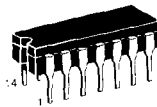




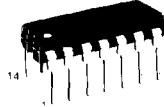
### B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

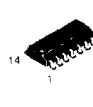
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices (Exceptions: MC14068B and MC14078B)



**L SUFFIX**  
CERAMIC  
CASE 632



**P SUFFIX**  
PLASTIC  
CASE 646



**D SUFFIX**  
SOIC  
CASE 751A

#### ORDERING INFORMATION

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBD SOIC

T<sub>A</sub> 55 to 125 C for all packages.

#### MAXIMUM RATINGS\* (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient) per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	65 to +150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

**MC14001B**  
Quad 2-Input NOR Gate

**MC14002B**  
Dual 4-Input Nor Gate

**MC14011B**  
Quad 2-Input NAND Gate

**MC14012B**  
Dual 4-Input NAND Gate

**MC14023B**  
Triple 3-Input NAND Gate

**MC14025B**  
Triple 3-Input NOR Gate

**MC14068B**  
8-Input NAND Gate

**MC14071B**  
Quad 2-Input OR Gate

**MC14072B**  
Dual 4-Input OR Gate

**MC14073B**  
Triple 3-Input AND Gate

**MC14075B**  
Triple 3-Input OR Gate

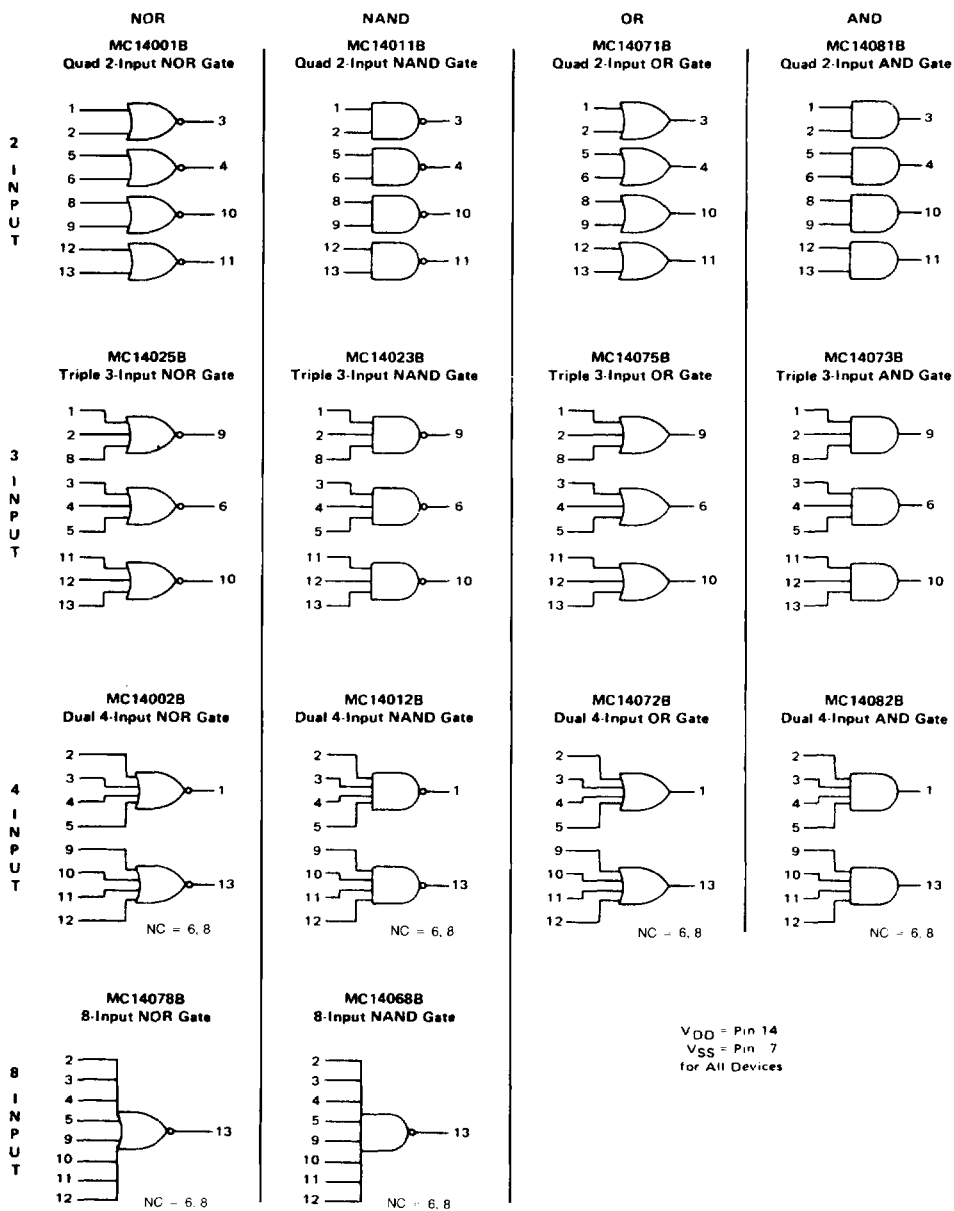
**MC14078B**  
8-Input NOR Gate

**MC14081B**  
Quad 2-Input AND Gate

**MC14082B**  
Dual 4-Input AND Gate

# CMOS B-SERIES GATES

## LOGIC DIAGRAMS

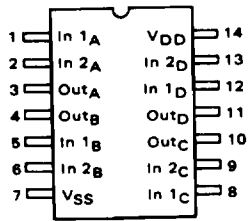


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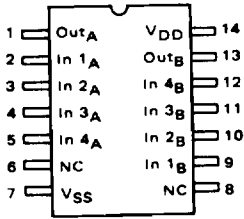
# CMOS B-SERIES GATES

## PIN ASSIGNMENTS

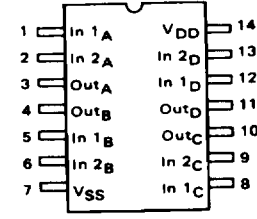
**MC14001B**  
Quad 2-Input NOR Gate



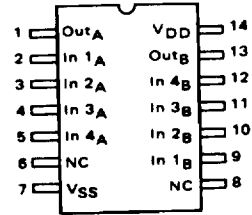
**MC14002B**  
Dual 4-Input NOR Gate



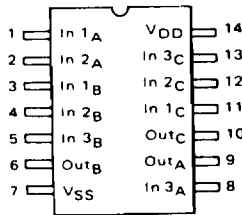
**MC14011B**  
Quad 2-Input NAND Gate



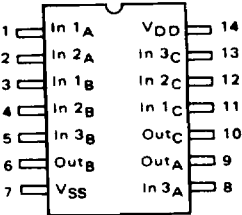
**MC14012B**  
Dual 4-Input NAND Gate



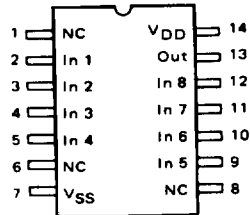
**MC14023B**  
Triple 3-Input NAND Gate



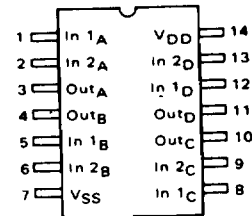
**MC14025B**  
Triple 3-Input NOR Gate



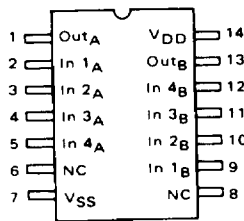
**MC14068B**  
8-Input NAND Gate



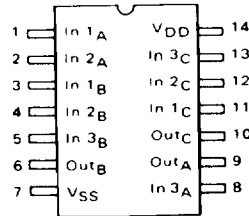
**MC14071B**  
Quad 2-Input OR Gate



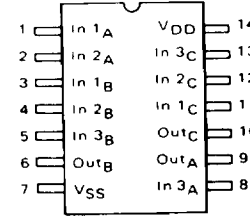
**MC14072B**  
Dual 4-Input OR Gate



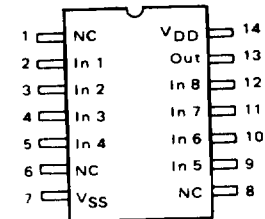
**MC14073B**  
Triple 3-Input AND Gate



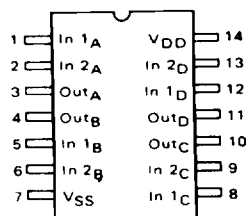
**MC14075B**  
Triple 3-Input OR Gate



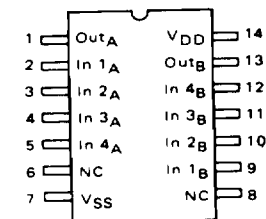
**MC14078B**  
8-Input NOR Gate



**MC14081B**  
Quad 2-Input AND Gate



**MC14082B**  
Dual 4-Input AND Gate



NC = No Connection

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# CMOS B-SERIES GATES

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C <sub>L</sub> = 50 pF)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub> /N							μAdc
		10	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> /N							
		15	I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub> /N							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

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# CMOS B-SERIES GATES

## B-SERIES GATE SWITCHING TIMES

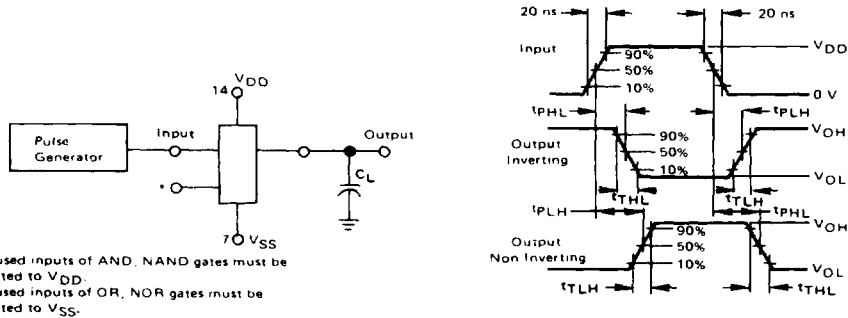
SWITCHING CHARACTERISTICS\* ( $C_L = 50 \text{ pF}$ ,  $T_A \approx 25^\circ \text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ #	Max	Unit
Output Rise Time, All B-Series Gates $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time, All B-Series Gates $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time MC14001B, MC14011B only $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 27 \text{ ns}$ All Other 2, 3, and 4 Input Gates $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$ 8-Input Gates (MC14068B, MC14078B) $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —	125 50 40  160 65 50  200 80 60	250 100 80  300 130 100  350 150 110	ns

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

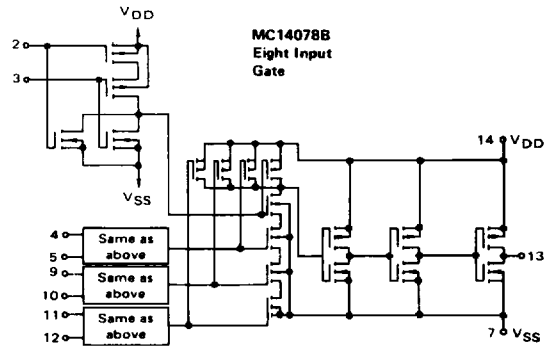
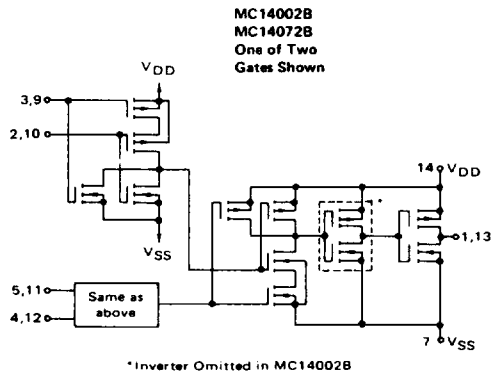
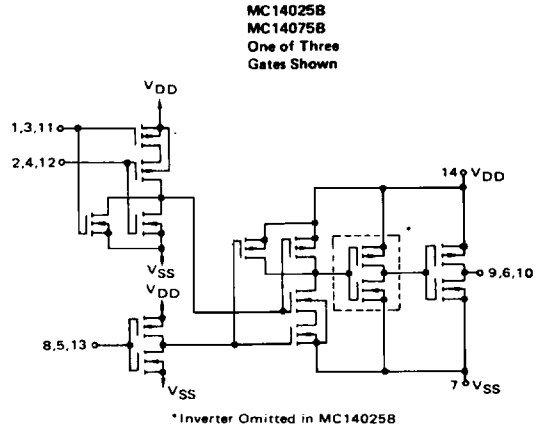
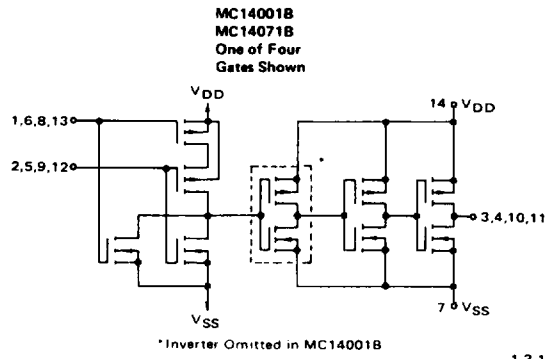


\*All unused inputs of AND, NAND gates must be connected to  $V_{DD}$ .  
 All unused inputs of OR, NOR gates must be connected to  $V_{SS}$ .

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# CMOS B-SERIES GATES

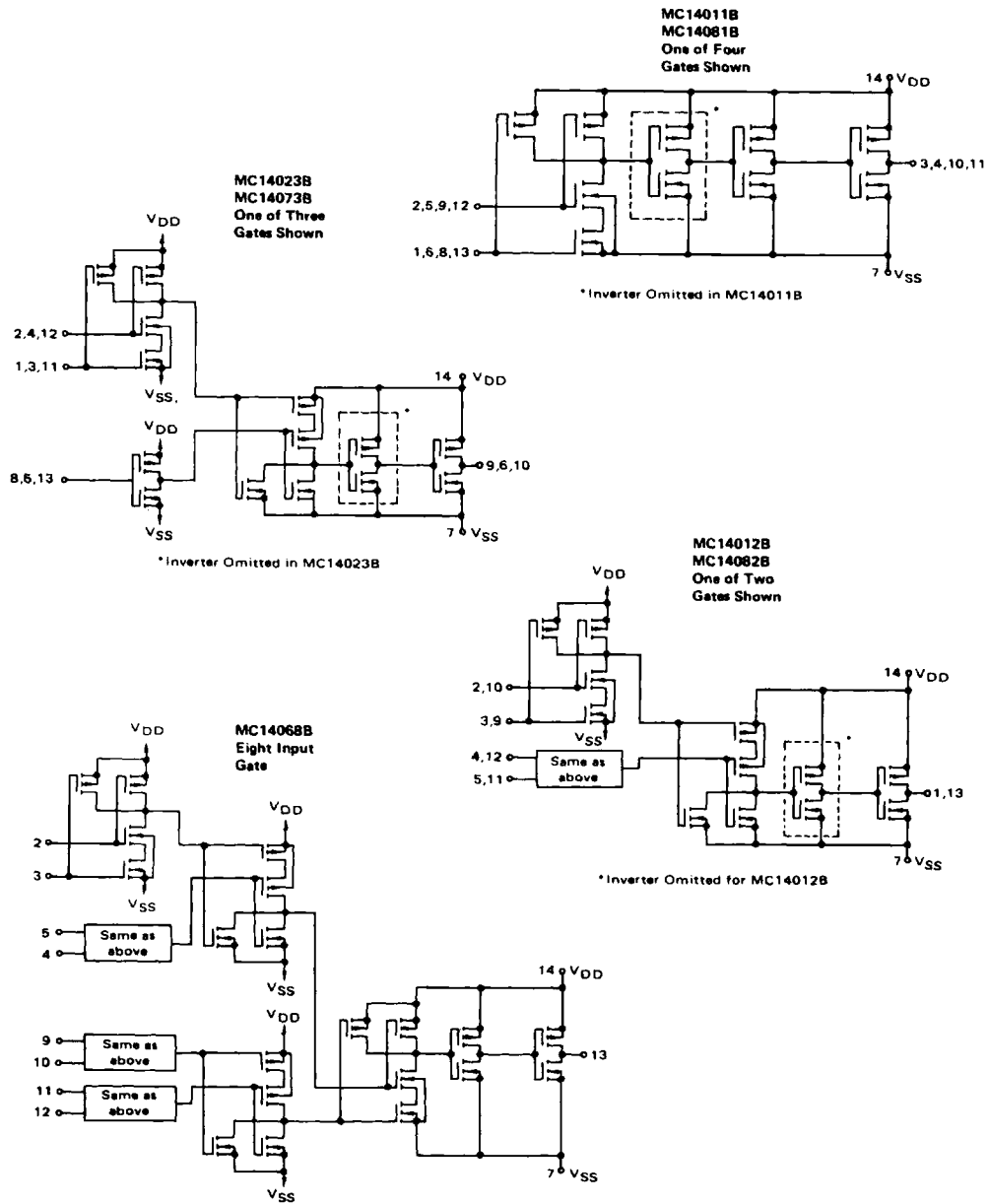
## CIRCUIT SCHEMATIC NOR, OR Gates



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# CMOS B-SERIES GATES

## CIRCUIT SCHEMATICS NAND, AND Gates



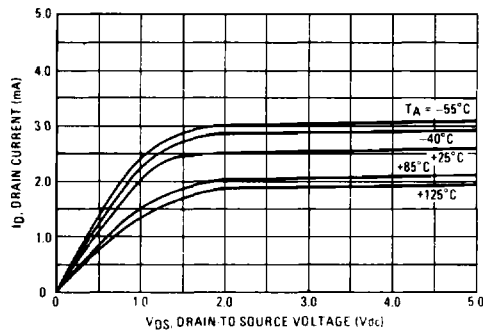
6

# CMOS B-SERIES GATES

## TYPICAL B-SERIES GATE CHARACTERISTICS

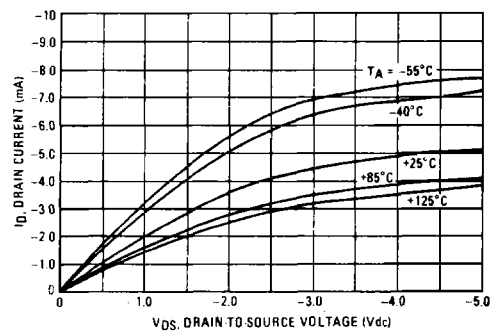
**N-CHANNEL DRAIN CURRENT (SINK)**

**FIGURE 2 –  $V_{GS} = 5.0$  Vdc**

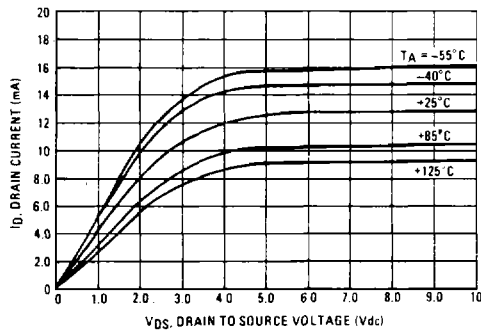


**P-CHANNEL DRAIN CURRENT (SOURCE)**

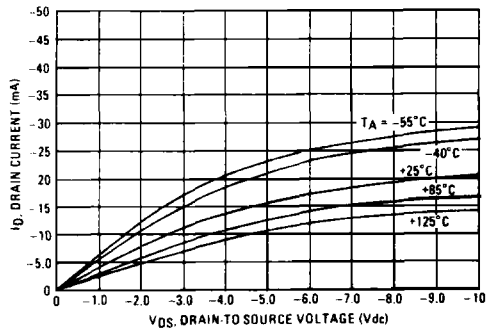
**FIGURE 3 –  $V_{GS} = -5.0$  Vdc**



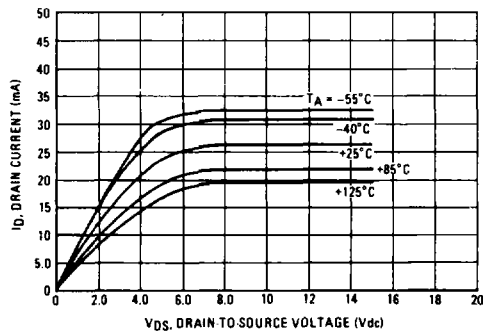
**FIGURE 4 –  $V_{GS} = 10$  Vdc**



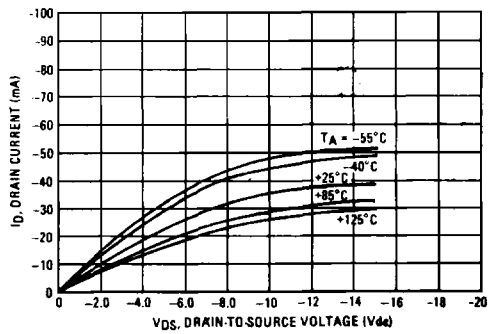
**FIGURE 5 –  $V_{GS} = -10$  Vdc**



**FIGURE 6 –  $V_{GS} = 15$  Vdc**



**FIGURE 7 –  $V_{GS} = -15$  Vdc**



These typical curves are not guarantees, but are design aids.  
Caution: The maximum rating for output current is 10 mA per pin.

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# CMOS B-SERIES GATES

## TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

### VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 -  $V_{DD} = 5.0 \text{ Vdc}$

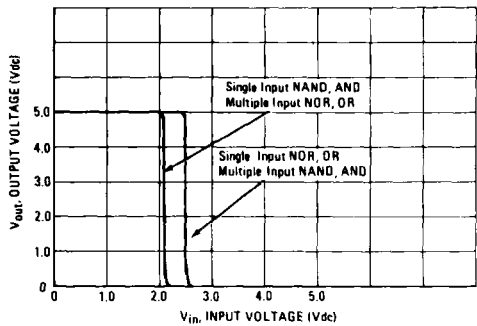


FIGURE 9 -  $V_{DD} = 10 \text{ Vdc}$

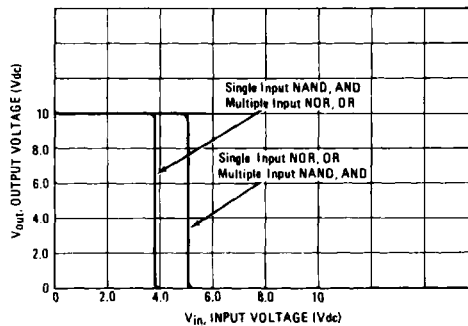
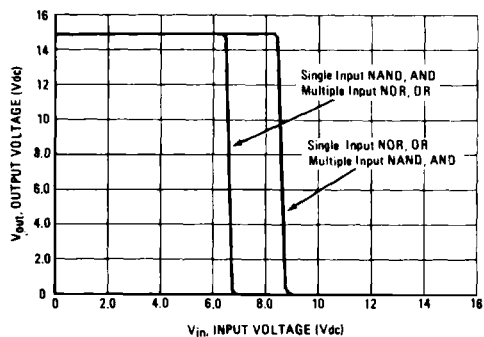


FIGURE 10 -  $V_{DD} = 15 \text{ Vdc}$



### DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values  $V_{IL}$  and  $V_{IH}$  for the output(s) to be at a fixed voltage  $V_O$  are given in the Electrical Characteristics table.  $V_{IL}$  and  $V_{IH}$  are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

- 1.0 V with a 5.0 V supply
- 2.0 V with a 10.0 V supply
- 2.5 V with a 15.0 V supply

FIGURE 11 - DC NOISE IMMUNITY

